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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/025,289	12/19/2001	Andrew K. Martin	SC11522TS	1877

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EXAMINER	
THOMPSON, ANNETTE M	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 03/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/025,289	MARTIN ET AL.	
	Examiner	Art Unit	
	A. M. Thompson	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicants' Amendment to 10/025,289 has been examined. Claims 9 and 16 are amended. Claims 1-26 are pending.

1. Applicants' amendment obviates the claims objections but it is otherwise unpersuasive. The rejections of the prior office actions are therefore incorporated herein.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Rejection of claims 1-18 and 21-25

3. Claims 1-18 and 21-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Martin et al. (Martin), U.S. Patent 6,378,112. Martin discloses a method of verification of design blocks and a method of equivalence checking of multiple design views.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in

the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

4. Pursuant to claim 1, Martin teaches a verification system (see Abstract) comprising a representation of a first design representing a specification having a predetermined functionality (Fig. 2, #202); a representation of a second design, the representation of the second design intended to satisfy the predetermined functionality of the first design (Fig. 2, #204) , the verification system functioning to affirm that the representation of the second design satisfies the predetermined functionality of the representation of the first design (col. 2, ll. 15-29) ; a plurality of design inputs (Fig. 1, #122, #124); a tester for comparing the representation of the second design with the representation of the first design (Fig. 2, #210) and detecting when the representation of the second design does not satisfy the representation of the first design (Fig. 2, #214), the tester providing a failure indicator and a characterization of a failure in response to the detecting, the tester further comprising a failure analyzer for applying one or more constraints to the characterization of the failure, the one or more constraints representing restrictions on permissible test parameters of the second design representation, and determining whether the one or more constraints will prevent the failure from occurring (col. 6, ll. 1-11).

5. Pursuant to claim 2, wherein the verification system affirms that the second design is functionally equivalent to the first design (col. 3, ll. 22-26).

6. Pursuant to claims 3 -5, wherein one of the first design or the second design is an RTL representation and the other is a gate level representation or one of the first or

the second design is an RTL representation and the other is a transistor level representation or the representation of the first design and the representation of the second design are two different representations of a same design (col. 2, ll. 14-43).

7. Pursuant to claim 6, wherein the constraints are supplied as design inputs (Fig. 2, col. 2, ll. 15-29).

8. Pursuant to claim 7, wherein the constraints are supplied by a user of the verification system (Claim 8, claim 15).

9. Pursuant to claim 8, wherein the constraints originate from the tester (the symbolic assertion generation module, col. 2, line 63 to col. 3, line 31).

10. Pursuant to claim 9, wherein the first and second designs represent a portion of an integrated circuit design that is less that all of the integrated circuit design. . .(Fig. 2, #200 cols. 2-3).

11. Pursuant to claim 10, wherein the one or more constraints further comprise a set of constraints and an order in which the set of constraints is applied is dependent upon the characterization of the failure (col. 5, ll. 41-67).

12. Pursuant to claim 11, wherein not every constraint is applied to the characterization of the failure ((col. 5, ll. 41-67).

13. Pursuant to claim 12, wherein the one or more constraints are generated by any of the following comprising creation of cutpoints in the representation of the first and second designs; input signals external to the first and second design representations; or state-holding elements contained within the representation of the first design and second design (col. 3, line 32 to col. 4, line 20).

14. Pursuant to claim 13, a method of verifying functional similarity (see Abstract) between a first design and a second design intended to satisfy functionality of the first design, comprising receiving a representation of the first design (Fig. 2, #202); receiving a representation of the second design (Fig. 2, #204); receiving a plurality of design inputs (Fig. 1, #122, #124); executing a test program on a computer that compares the representation of the second design with the representation of the first design, and detecting when the representation of the second design does not satisfy the representation of the first design (Fig. 2, #210), the test program providing a failure indicator and a characterization of a failure in response to the detecting (Fig. 2, #214), the test program further comprising applying one or more constraints to the characterization of the failure, the one or more constraints representing restrictions on permissible test parameters of the second design representation, and analyzing the failure by determining whether the one or more constraints will prevent the failure from occurring (col. 6, ll. 1-11).

15. Pursuant to claim 14, further comprising affirming that the second design is fully functionally equivalent to the first design (col. 3, ll. 22-26).

16. Pursuant to claim 15, further comprising obtaining the one or more constraints that are applied to the characterization of the failure as a portion of the plurality of design inputs that are received failure (col. 5, ll. 41-67).

17. Pursuant to claim 16 further comprising permitting another design separate from the first design and the second design to determine the one or more constraints .(Fig. 2, #200 cols. 2-3).

18. Pursuant to claim 17, wherein a set of constraint is created and predetermined one of the sets of constraints are applied depending upon the characteriation of the failure (col. 5, ll. 41-67).

19. Pursuant to claim 18, further comprising generating the one or more constraints by having constraints associated with cutpoints created in the representation of the first and second designs; input signals external to the first and second design representations; or state-holding elements contained within the representation of the first design and second design (col. 3, line 32 to col. 4, line 20).

20. Pursuant to claim 21, this independent claim incorporates the limitations already rejected in claim 1, supra, and additionally includes the limitation of a symbolic stimulus generator that analyses the representation of the first design to determine a set of inputs to a test point and generates a set of symbolic stimulus to be applied to corresponding test point inputs in the representation of the second design. Martin discloses this limitations at Fig. 2, #210; col. 2, line 63 to col. 3, line 67). Therefore claim 21 is likewise rejected.

21. Pursuant to claim 22 and 25, wherein the finding of additional inputs corresponding to additional nodes comprises tracing from an output-to- input direction through the representation of the first design to identify the additional inputs (col. 5, ll. 27-67).

22. Pursuant to claim 23, wherein the corresponding inputs in the representation of the second design do not structurally exist but functional correspondence exists (col. 2, ll. 15-43).

23. Pursuant to claim 24, this independent claim incorporates the limitations already rejected in claim 1, supra, and additionally includes the limitation of a symbolic stimulus generator that analyses the representation of the first design to determine a set of inputs to a test point and generates a set of symbolic stimulus to be applied to corresponding test point inputs in the representation of the second design. . .. Martin discloses these additional limitations at Fig. 2, #210; col. 2, line 63 to col. 3, line 67. Therefore claim 24 is likewise rejected.

24. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Rejection of claims 19, 20 and 26

25. Claims 19, 20, and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Pixley et al., U.S. Patent 5,754,454. Pixley discloses a method for determining functional equivalence between design models.

26. Pursuant to claim 19, Pixley discloses a computer readable storage medium, for storing a verification system (claim 27; col. 8, 29-32) comprising a set of instruction that executes receiving a representation of a first design. . . (Fig. 1); receiving a representation of a second design. . . (Fig. 1); receiving a plurality of inputs (col. 3, ll. 12-17); comparing the first and second design representations. . .(col. 2, ll. 35-57) . .applying one or more constraints to the characterization of the failure. . .(col. 5, ll. 38-65).

27. Pursuant to claim 20 further comprising maintaining the one or more constraints in a list that is applied in an order based upon the failure characterization (col. 6, ll. 5-64).

28. Pursuant to claim 26, this independent claim incorporates the limitations already rejected by claim 19 and further includes the limitation of a symbolic stimulus generator also disclosed by Pixley (the BDD creations, col. 2, ll. 35-57). Therefore, claim 26 is likewise rejected.

Remarks

29. Applicants point out that Applicants' disclosure discusses the use of additional nodes; however Applicants' claim 1 does not recite the limitation of additional nodes. Therefore, Applicants may not rely on this point in asserting patentability of at least claim 1 in the instant Application over Martin et al.. Independent claims 21 and 24 recite this limitation and it is disclosed in Martin at fig. 2, #206 which necessarily includes additional nodes, (cf. Applicants' Fig. 1, #106, the parenthetical information). With respect to the elements of claim 1, Martin discloses the limitations of claim 1 to the same extent as Applicants' disclosure. For example, Applicants' disclosure **does not** teach a failure analyzer for applying one or more constraints so in lieu of applying a 35 U.S.C. 112, first paragraph rejection to the claim, Examiner interpreted that limitation and provided cites accordingly. Martin discloses a tester (Fig. 2, #208, 210). Further, Martin, col. 6, lines 1-16 discloses the limitation of a failure indicator (Martin discloses the use of an identity match (col. 6, ll. 5-13) and a characterization of the failure (col. 6, ll. 16-18). Martin also discloses a symbolic stimulus generator (Fig. 2, #208).

30. Applicants define characterization of a failure (specification, page 10, lines 14-20) as comparing the expected functionality and the actual functionality to obtain a failure condition. Pixley compares cutpoint pairs to determine equivalence (col. 5, line 66 to col. 6, line 4). Then Pixley outputs a result (XOR model output equals one or zero) to indicate whether or not an identity has been determined. This resulting output of Pixley is at least similar if not equivalent to Applicants' failure condition and Pixley's entire process of determining equivalence reads on Applicants' failure characterization process.

31. Pixley's cutpoint variables represent constraints which are substituted into an XOR model to determine a failure condition, column 6, lines 25-40 (Applicants' characterization of a failure). Variables (constraints) are substituted and it is determined which variables result in failure. This process is similar if not equivalent to Applicants' limitation of determining whether the constraints will prevent a failure from occurring. Pixley's passage citing removal of invalid output variables was introduced to illustrate that the process of determining equivalence or characterizing a failure exists in Pixley, otherwise there would be no determination of invalidity and subsequent removal. At column 5, lines 55-58, Martin discloses the **determination** of invalid cutpoint pairs. This sort of determination would necessarily require an indication of failure or success, i.e. a failure indicator.

32. Pixley's method relates to semiconductor device verification, column 1, lines 5-9. Pixley's ATPG generates symbolic stimuli to apply to the BDD design representations.

Conclusion

33. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

34. Any inquiry concerning this communication or earlier communications should be directed to Examiner A.M. Thompson whose telephone number is (571) 272-1909. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 4:30 p.m.. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matthew S. Smith, can be reached on (571) 272-1907.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-1562 or the Customer Service Center whose telephone number is (571) 272-1750.

35. Responses to this action should be mailed to the appropriate mail stop:

Mail Stop _____
Commissioner for Patents
P.O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

(703) 872-9306, (for all **OFFICIAL** communications intended for entry)

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